	Application No.	Applicant(s)
	10/693,576	LEWIS ET AL.
Notice of Allowability	Examiner	Art Unit
	Tan V. Mai	2193
The MAILING DATE of this communication appe All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RI of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in this app or other appropriate communication GHTS. This application is subject to	olication. If not included will be mailed in due course. THIS
1. \boxtimes This communication is responsive to <u>5/19, 9/9 & 10/24/05</u> .		
2. The allowed claim(s) is/are <u>1-56</u> .	,	
3.	been received. been received in Application No cuments have been received in this communication to file a reply ENT of this application. itted. Note the attached EXAMINER es reason(s) why the oath or declara t be submitted. on's Patent Drawing Review (PTO- as Amendment / Comment or in the Comment or in the Comment or in the Comment of the drawing he header according to 37 CFR 1.121(complying with the requirements 'S AMENDMENT or NOTICE OF tion is deficient. 948) attached Office action of the back) of d).
Attachment(s) 1. ☑ Notice of References Cited (PTO-892) 2. ☑ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☑ Information Disclosure Statements (PTO-1449 or PTO/SB/0 Paper No./Mail Date 10/23/03 & 6/7/04 4. ☑ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. Notice of Informal P 6. Interview Summary Paper No./Mail Dat 8), 7. Examiner's Amendr	Patent Application (PTO-152) (PTO-413), te ment/Comment ent of Reasons for Allowance Tan V. Mai
		Primary Examiner

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REASON FOR ALLOWANCE

1. The following is an examiner's statement of reasons for allowance: the recorded references do NOT teach or suggest: (1) the logic element having the combination of LUTs, pass gates, inverters & carry chain unit for providing either the logic mode or arithmetic mode as recited in independent claim 1; (2) the logic element having the combination of LUTs, multiplexers & XOR unit(s) for providing either the logic mode or arithmetic mode as recited in independent claims 8,15, 22, 29 and 36; (3) the logic element having the combination of LUTs, multiplexers & adder unit for providing either the logic mode or arithmetic mode as recited in independent claim 43; and (4) the logic element having the combination of LUTs, a plurality of types of multiplexers & carry-out select multiplexer for providing either the logic mode or arithmetic mode as recited in independent claim 50.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

- 2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Cited references are art of interested.
- 3.. Any inquiry concerning this communication or earlier communications from the

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examiner should be directed to Tan V. Mai whose telephone number is (571) 272-3726. The examiner can normally be reached on Mon-Wed and Fri. from 9:30am to 2:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki, can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is:

Official

(571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Tan V. Mai Primary Examiner